

ABSTRACT OF THE DISCLOSURE

A method for erasing a bit of a memory cell in a non-volatile memory cell array, the method comprising applying an erase pulse to at least one bit of at least one memory cell of the array, waiting a delay period wherein a threshold voltage of the at least one memory cell drifts to a different magnitude than at the start of the delay period, and after the delay period, erase verifying the at least one bit to determine if the at least one bit is less than a reference voltage level.